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MONOLITHIC GaAs DUAL-GATE FET PHASE SHIFTER

RCA Laboratories
Princeton, New Jersey 08540

MAY 1981

TRI-ANNUAL REPORT NO. 2
for the period 1 January 1981 to 30 April 1981

Prepared for
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Progress is reported:

(1) The photomask of a 0 to 90 deg monolithic GaAs dual-gate FET phase shifter was designed and ordered from Photronics Labs, Inc. in Connecticut. The estimated delivery date is late June 1981.

(2) A technique for fabricating "via" holes using laser drilling was developed. This technique can drill a 1-mil-diameter via hole → cont

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through a 4-mil-thick GaAs substrate without much undercut and without an infrared microscope for backside alignment.

(3) A four-way, in-phase combiner on Al_2O_3 substrate has been developed with good performance. The same design is being modified for fabrication on GaAs semi-insulating substrates. This four-way, in-phase combiner is needed for the 0 to 360° phase shifter that will be developed in the next phase.

Technical Problems

There was no major problem during this period.

PREFACE

This Tri-annual Report describes the work performed under Contract No. N00014-79-C-0568, 1 January 1981 to 30 April 1981, in the Microwave Technology Center, F. Sterzer, Director, H. C. Huang is the project supervisor, and M. Kumar is the project scientist.

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I. Objective

The objective of this four-year program (Sept. 1, 1979 to Aug. 31, 1983) is to develop a monolithic GaAs dual-gate FET phase shifter, operating over the 4- to 8-GHz frequency band and capable of a continuous programmable phase shift from 0° through N times 360° where N is an integer. The phase shift is to be controllable to within +3°. This phase shifter will be capable of delivering an output power up to 0 dBm with an input and output VSWR of less than 1.5:1.

II. Progress

In the last tri-annual report, for the period 1 September 1980 to 31 December 1980, we reported the development of a 360° GaAs dual-gate FET phase shifter using discrete components. The 360° phase shifter consists of two 90° phase shifters, a 180° hybrid, and a in-phase power combiner. The development of a truly monolithic 360° phase shifter will require all the components to be monolithically integrated on a single GaAs substrate. To achieve a 360° phase shifter, we are developing the individual components in this phase and will integrate the above-mentioned components on GaAs substrates in the next phase (1982). The development of a 360° phase shifter will require the following:

(1) 90° monolithic dual-gate GaAs phase shifters
(2) monolithic 180° hybrid
(3) monolithic in-phase combiner

We have already demonstrated a 180° hybrid on an Al_2O_3 substrate (Bimonthly Report No. 6) and a monolithic dual-gate FET amplifier (Bimonthly Report No. 3).

A. Development of a 90° Monolithic GaAs Dual-Gate FET Phase Shifter

The goals for the second phase of this program are to develop and demonstrate a 0 to 90° monolithic phase shifter. During this tri-annual report period 1 January 1981 to 30 April 1981, we have completed the design of a monolithic GaAs dual-gate FET phase shifter. The drawings have been sent to Photronic Labs, Inc. (Danbury, CT) which will prepare the photomasks. The 90° monolithic phase shifter includes, on the same GaAs substrate, the following components: dual-gate FETs, matching circuits, interdigitated 90° hybrid, in-phase power combiner, airbridges, thin film resistor, MIM capacitors for

bypassing the shunt-matching elements and injecting the bias to the dual-gate FET, and "via" holes for low inductance ground connection of FET sources and capacitors. The masks are expected to be delivered in June 1981.

We are in the process of fabricating the 90°, interdigitated hybrids on 100-μm-thick GaAs substrates.

B. "Via" Hole Technique

A truly monolithic microwave integrated circuit requires the grounding of source pads, shunt capacitors, etc., through "via" holes at their appropriate locations on the GaAs chip. We have developed a technique of fabricating "vias" by front-side alignment. Chemically etched "vias" have been used and reported in literature for monolithic integrated circuits. There are distinct disadvantages and difficulties with this technique:

(1) The backside alignment is difficult and requires the use of expensive equipment such as an infrared aligner.

(2) Chemical etching produces considerable undercutting making the holes much larger than those defined by the hole pattern (Fig. 1). Furthermore, not all the holes are etched at the same rate.

(3) Laser drilling of the holes directly on the surface of GaAs produces extensive damage on the surface (Fig. 2).

Figure 1. Chemical etch. Diameter of the original hole pattern is 25 μm. 500X.

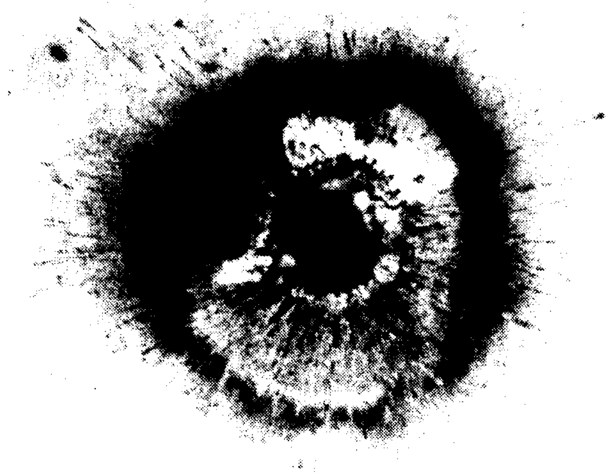

Figure 2. Laser drill without photoresist. 500A.

We have developed a technique which avoids the difficult backside alignment and nonuniform chemical etch. Although a laser is used to drill the holes, our technique involves the use of a photoresist protective layer to minimize surface damage.

The following is the step-by-step procedure.

(1) The device with the circuits is fabricated on the front side of the GaAs wafer which is 10 mil thick. It is much easier to process a 10-mil-thick wafer than, say, a 4-mil wafer.

(2) After the front-side-device process is completed, the wafer is thinned down to the desired thickness (about 4 mil) from the back side by suitable mechanical and chemical means.

(3) The front surface is coated with 1- to 2-μm-thick photoresist and the hole pattern is defined. This minimizes the surface damage by laser.

(4) Holes are drilled using a laser. A power setting of 25 to 30 kW is found to be adequate to drill 1-mil-diameter holes in a 4-mil (100 μm) thick GaAs wafer.

(5) Figure 3 shows the front view of the hole after removing the photoresist. It can be seen that the diameter of the hole is about 35 to 40 μm. (The original hole pattern was 25 μm in diameter.)

(6) Cr (∿500 Å) and Au (∿3000 Å) are evaporated on the backside of the wafer. Electrical plating up through the holes is carried out.

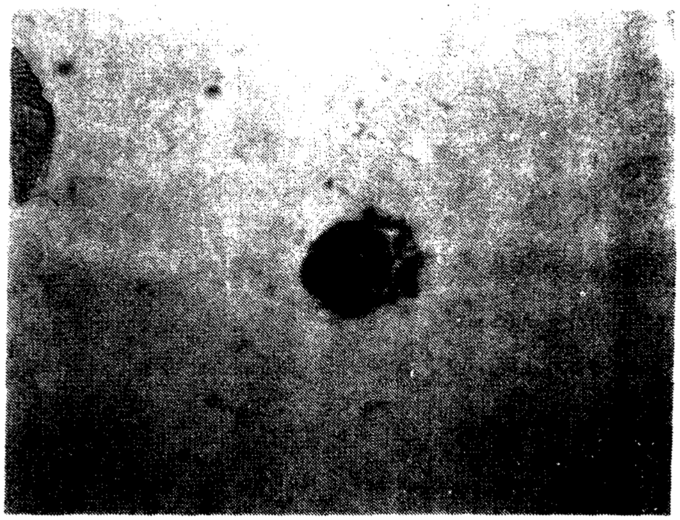

Figure 3. Laser drill. Diameter of the original hole pattern is 25 μm. 500X.

C. Development of a Four-Way, In-Phase Power Divider/Combiner

We have developed a planar, four-way, in-phase power divider/combiner. This four-way, in-phase combiner is required for combining four outputs of the dual-gate FET amplifiers in a 360° phase shifter (Tri-annual Report No. 1). The divider/combiner reported here was fabricated on alumina substrate and is compatible for monolithic integration on GaAs substrates with other passive and active components.

Figure 4 shows the schematic of a planar, four-way, in-phase power divider/combiner on Al_2O_3 substrate. The input is split into four outputs through four $\lambda/4$ sections of the transmission lines. The impedance of each $\lambda/4$ section of line is 100 Ω and the value of the isolation resistance is 70.7 Ω. The input

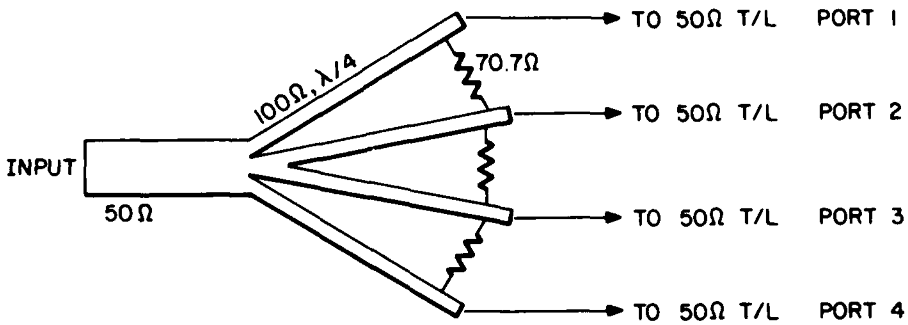

Figure 4. Schematic of a planar four-way power divider/combiner.

and output impedances are 50 Ω each. The performance of the divider/combiner is shown in Figs. 5 through 8. Figure 5 shows the variation of coupling at four output ports with frequency. Figure 6 presents the isolation vs frequency between any two ports. The isolation is better than 13 dB over the band. The insertion loss and return loss of the divider/combiner are presented in Figs. 7 and 8. The overall phase variation between the ports is $\pm 6°$.

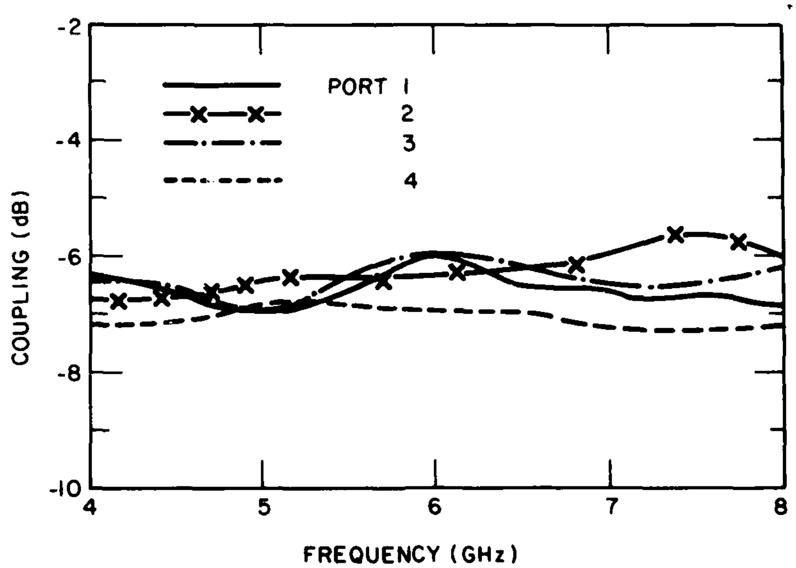

Figure 5. Variation of coupling with frequency.

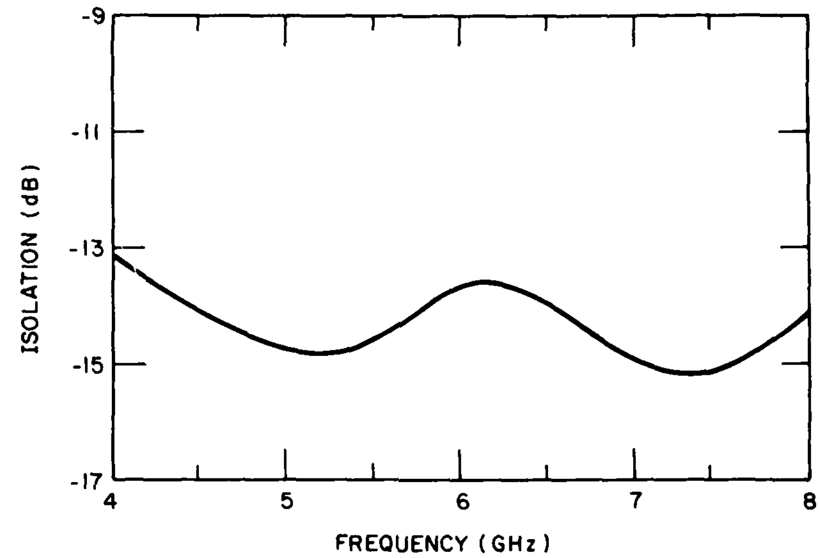

Figure 6. Variation of isolation between ports with frequency.

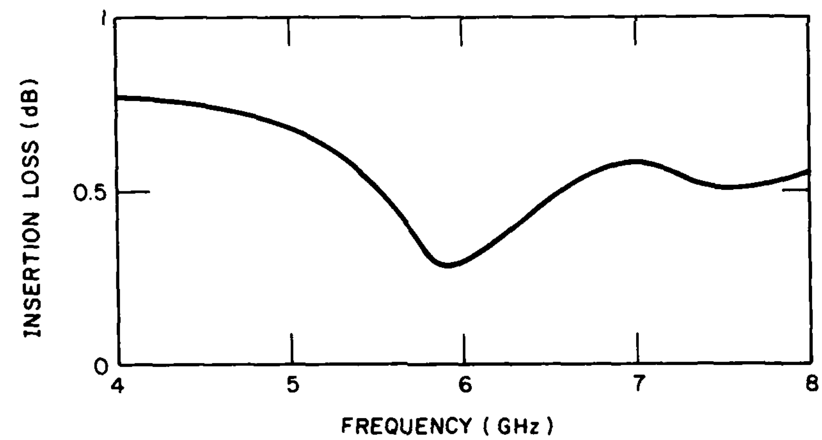

Figure 7. Variation of insertion loss with frequency.

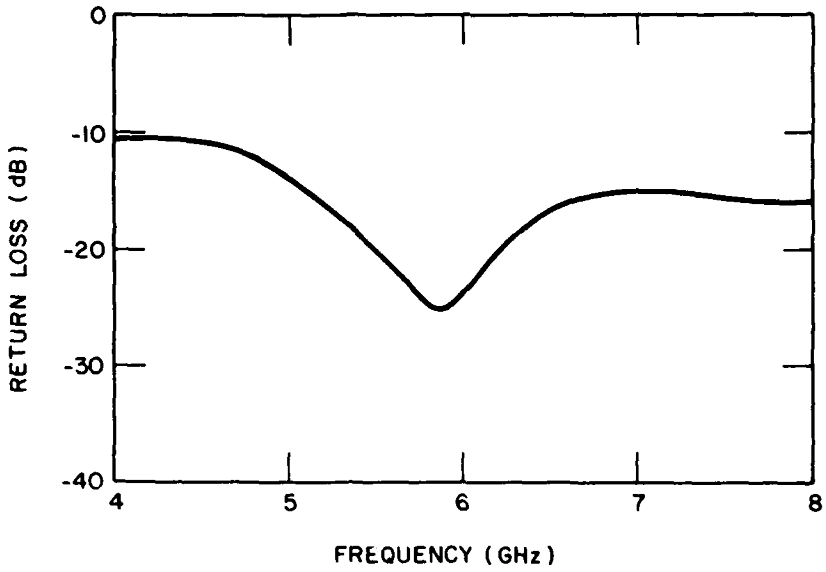

Figure 8. Variation of return loss with frquency.

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